CENG 450

Post-lab Summary

February 25th, 2014

Lab Session 4

In session 3, we finished connecting our processor modules, and began testing a-type instructions. We were also able to begin designing the program counter, controller and memory. The testing was done using the code provided in class, however we did insert NOPs since hazard handling has not yet been implemented. In addition, we included the register values in the initialization of the register module since L-type instructions have not yet been implemented. After some troubleshooting, the majority of which involved syntax, we were able to verify that our design executed the code properly.

The next step, we planned was to implement the program counter. The PC would consist of a counter, an EN pin, CLK pin, BR pin, input bus, and bus or pin. In this setup, the EN pin can be used to keep the PC from incrementing if the pipeline is stalled, and the B-type instructions can pass branch destinations using the input bus and BR pin. The output will then connect to memory so that the correct instruction can be retrieved. At some point, the effective address needs to be translated into an actual address. This will likely be done in the PC.